

ACTIVE MATRIX DISPLAY DRIVING CIRCUIT

FIELD OF THE INVENTION

This invention relates to a driving circuit of electro-luminescence device (EL device) is applicated in
5 pixel of display. More particularly, the invention is directed to a driving device that improves the defect of images on an active matrix Poly-Si TFT EL device resulted from an inconsistent threshold voltage (V_{th}) and IR drop in addition to charging/discharging time problem.

BACKGROUND OF THE INVENTION

An EL device display can be classified according to its driving method, passive matrix (PM-EL Display) and active matrix (AM-EL Display). AM-EL display uses TFT (Thin Film Transistor) with a capacitor for storing data
15 signals that can control EL display gray levels of brightness.

The manufacturing procedure of a PM-EL display is simpler in comparison and less costly; however, it is limited in its size (< 5 inches) because of its driving
20 mode and has a lower-resolution display application. In order to produce an EL display with higher resolution and larger size, utilizing active-matrix driving is necessary. The AM-EL uses TFT with a capacitor for storing data signals, so that the pixels can maintain their brightness
25 after line scanning; on the other hand, pixels of passive

matrix drive only light up when the scan line selects them. Therefore, with active matrix driving, the brightness of EL device is not necessarily ultra-bright, resulting in longer lifetime, higher efficiency and higher resolution.

- 5 Naturally, EL devices with active matrix driving are suitable for display applications of a higher resolution and excellent picture quality.

LTPS (Low Temperature Poly-Silicon) and a-Si (Amorphous Silicon) are both technologies of TFT
10 integrating on glass substrate. The obvious differences are electric characteristics and complexity of processing. Although LTPS-TFT possesses higher carrier mobility and higher mobility means more current can be supplied, the process is much more complex. However, the process
15 of a-Si TFT is simpler and more mature, except for low carrier mobility. Therefore, a-Si process has better competitive advantage in cost.

Due to limitations of LTPS process capability, threshold voltage (V_{th}) and mobility of TFT elements
20 produced vary leading to different properties of each TFT element. When the driving system achieves gray scale by analog voltage modulation, an EL device produces a different output current despite having the same data voltage signal input due to the different TFT
25 characteristics of various pixels. Therefore, the

luminance of an OLED varies. Images of erroneous gray scale will show up on OLED panel and seriously damage image uniformity.

5 The most urgent problem of the AM-EL display to be solved currently is how to reduce the impact of uneven LTPS-TFT characteristics. Such an issue requires an immediate solution for follow-up development and applications since images on the display tell the difference.

10 U.S. Pat. No. 6,373,454 discloses 「Active matrix electroluminescent display devices」 (Apr. 26, 2002), No. 6,229,506 discloses 「Active matrix light emitting diode pixel structure and concomitant method」 (May 26, 2001) and Toshiba publishes a thesis titled 「A Novel Current
15 Programmed Pixel for Active Matrix OLED Displays」 (Society for Information Display 2003 (SID 2003)) .

For the above patents and thesis, the input current on the data line and output current to the EL device was 1:1. Thus, there was a defect of long charge/discharge times
20 for the capacitor and the parasitical capacitor at low current input.

U.S. Pat. No. 6,359,605 discloses 「Active matrix electroluminescent display devices」 (Mar. 26, 2002), Pat. No. 6,501,466 proposes 「Active matrix type display
25 apparatus and drive circuit thereof」 (Dec. 26, 2002) and

Pat. No. 6,535,185 presents 「Active driving circuit for display panel」 (Mar. 26, 2003).

For the aforementioned patents, the theory of current mirror is utilized to achieve the rate of input current and output current as $n:1$. However, two TFTs in the current mirror have to be matched to prevent threshold voltage (V_{th}) difference and mobility. Thus, requirements for TFT manufacturing process are stricter.

The common problem for the circuits above is the voltage discharged from the storage capacitor to the gate and source of the driving transistor (V_{gs}) has to be less than the threshold voltage (V_{th}) of the driving transistor. Nevertheless, V_{gs} is larger than V_{th} due to long discharging time. Consequently, EL device illuminates via a small current and therefore the contrast of the display panel is not good.

A thesis with the subject of 「A New Current Programmable Pixel Structure for large-Size and High-Resolution AMOLEDs」 is released by Samsung (International Display Workshops 2002 (IDW 2002)). The theory of capacitive coupling is applied to change the gate voltage (V_g) of the driving TFT to establish a relationship between the output and input currents as $\text{output current} = A \times \text{input current} + B$ (A and B are constants). As capacitors are affected by the process or

the layout, the voltage of capacitive coupling changes and the output current of the driving transistor is influenced, too. Defects of this driving method are capacitance precision and impose strict requirements for capacitor processing and layout. In addition, the aperture ratio of pixels becomes smaller as two capacitors are required to drive one pixel.

SUMMARY OF THE INVENTION

The main purpose of this invention is to solve the said problems. This invention not only improves image defects resulting from uneven characteristics of TFT and IR drop, but also solves the problem of long charge/discharge times for low current inputs.

To achieve the objective above, every pixel on the display panel comprises one scan line and one data line. A driving device of each pixel includes a first scan transistor and a second scan transistor, whose gates (G) are connected to scan line and sources (S) connected to data line. A driving transistor is also included and connected to the voltage supply line.

The source (S) of connect transistor is connected to the drains (D) of the driving transistor and the second scan transistor and the gate (G) is connected to emission line.

The source (S) of first switch transistor is

connected to the first voltage supply and the gate is connected to the scan line; the source (S) of second switch transistor is connected to second voltage supply and the gate (G) is connected to the emission line.

5 One end of storage capacitor connects to the drains (D) of the first and second switch transistors and the other end is connected to the drain (D) of the first scan transistor and the gate (G) of the driving transistor. The anode of luminescence element is connected to the drain
10 of the connect transistor and the cathode is grounded. All transistors are PMOS transistors and the voltage of the second voltage supply is greater than that of the first voltage supply.

15 The first voltage supply can connect to the emission line and the second voltage supply connect to the scan line; alternatively, the first voltage supply can connect to the voltage supply; or, the first voltage supply can connect to the voltage supply and the second voltage supply connects to the scan line.

20 Another embodiment is to change all transistors to NMOS, and the driving circuit includes a first scan transistor and a second scan transistor, whose gates (G) connect to the scan line and sources (S) are connect to the data line. One driving transistor is also included, with
25 the source (S) grounded. One connect transistor is

included, with its source (S) connected to the drains (D) of the driving transistor and the first scan transistor and the gate (G) connected to one emission line.

5 The source (S) of one first switch transistor is connected to one first voltage supply and the gate (G) is connected to the scan line; the source (S) of the second switch transistor is connected to second voltage supply and the gate (G) is connected to the emission line.

10 One end of one storage capacitor connects to the drains (D) of the first and second switch transistors and the other end is connected to the drain (D) of the second scan transistor and the gate (G) of the driving transistor. The anode of one luminescence element is connected to the voltage supply and the cathode is connected to the
15 drain (D) of the connect transistor.

The same as the above driving circuit, the first voltage supply may be connected to the emission line and the second voltage supply connected to the scan line; alternatively, only the first voltage supply is grounded; or,
20 the first voltage supply is grounded and the second voltage supply is connected to the scan line.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is the circuit of a pixel in embodiment 1 in this invention.

25 FIG.2 is the circuit of a pixel in embodiment 2 in this

invention.

FIG.3 is the circuit of a pixel in embodiment 3 in this invention.

FIG.4 is the circuit of a pixel in embodiment 4 in this invention.

FIG.5 is the circuit of a pixel in embodiment 5 in this invention.

FIG.6 is the circuit of a pixel in embodiment 6 in this invention.

FIG.7 is the circuit of a pixel in embodiment 7 in this invention.

FIG.8 is the circuit of a pixel in embodiment 8 in this invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment 1:

Refer to Fig.1 for the circuit of a pixel of embodiment 1 in this invention. As the Figure shows: the driving circuit of each pixel on the display panel includes one scan line 10 and one data line 20 as follows:

Gates (G) of a first scan transistor T1 and a second scan transistor T2 connected to one scan line 10 and source (S) connected to a data line 20.

Source (S) of a driving transistor T3 connected to VDD. Source (S) of connect transistor T4 connected to

drains (D) of driving transistor T3 and second scan transistor T2 and gate(G) connected to one emission line 30.

Source (S) of a first switch transistor T5 connected
5 to first voltage supply V1 and gate(G) connected to scan line 10. Source (S) of a second switch transistor T6 connected to second voltage supply V2 and gate (G) connected to emission line 30. The above first scan transistor T1, second scan transistor T2, driving
10 transistor T3, connect transistor T4, first switch transistor T5 and second switch transistor T6 are PMOS transistors. One end of storage capacitor Cs connected to drains (D) of the first switch transistor T5 and second switch transistor T6 and the other end connected to drain(D) of
15 first scan transistor T1 and gate(G) of driving transistor T3. Anode of a luminescence device 40 connected to drain(D) of connect transistor T4 and cathode grounded. Luminescence device 40 is an electro-luminescence device (EL device).

20 Gates(G) of first scan transistor T1 and second scan transistor T2 controlled by nth Scan Line 10 and sources connected to data line 20.

Gate (G) of connect transistor T4 controlled by nth emission line 30. Current passing by luminescence device
25 40 determined by gate (G) of driving transistor T3.

Gate (G) of first switch transistor T5 controlled by nth scan line 10 and that of second switch transistor T6 controlled by nth emission line 30.

Actuation procedures of this invention are described
5 as follows:

1. When the system scans the nth scan line 10, the potential is low ($V_{S,L}$), leading first scan transistor T1, second scan transistor T2 and first switch transistor T5 to become on. As the potential of the nth emission line 30 is
10 high ($V_{E,H}$), connect transistor T4 and second switch transistor T6 are off. Thus, no current will pass through luminescence device 40 to prevent writing mistakes of storage capacitor Cs.

One end of storage capacitor Cs connected to gate(G)
15 of driving transistor T3 links up with data line 20 through scan transistor T1 and the other end is connected to first voltage supply V1 via first switch transistor T5. Meanwhile, part of data current I_{Data} charges/discharges storage capacitor Cs through first scan transistor T1 and
20 first switch transistor T5. Gate voltage (V_{g3}) of driving transistor T3 equals voltage of first voltage supply V1 less that of storage capacitor Cs ($V1 - V_{Cs}$).

Consequently, drive current (I_{Drive}) passing through driving transistor T3 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{sg3} -$
25 $V_{th3})^2$ (β as trans-conductance parameter of driving

transistor T3 and source gate voltage of driving transistor T3, $V_{sg3} = VDD - V_{g3} = VDD - (V1 - V_{CS})$. At present, data current I_{Data} equals current passing through storage capacitor C_s (I_{CS}) plus drive current (I_{Drive}) passing through driving transistor T3; i.e., $I_{Data} = I_{CS} + I_{Drive}$.

2. Voltage of storage capacitor C_s (V_{CS}) makes drive current (I_{Drive}) passing through driving transistor T3 the same as data current of data line 20; that is, $I_{Data} = I_{Drive} = (1/2) \times \beta \times (V_{sg3} - V_{th3})^2$ and $V_{sg3} = VDD - V_{g3} = VDD - (V1 - V_{CS})$.

Data write is completed at the moment and voltage of storage capacitor C_s (V_{CS}) = $(2 \times I_{Data} / \beta)^{(1/2)} - (VDD - V1 - V_{th3})$.

3. Lastly, when potential of the nth Scan Line 10 changes from low ($V_{S,L}$) to high ($V_{S,H}$), First scan transistor T1, second scan transistor T2 and first switch transistor T5 are off. Meanwhile, potential of the nth Emission line 30 changes from high ($V_{E,H}$) to low ($V_{E,L}$), leading connect transistor T4 and second switch transistor T6 to become on.

One end of storage capacitor C_s is connected to gate (G) of driving transistor T3 and the other end to second voltage supply V2 via second switch transistor T6. Thus, gate voltage V_{g3} of driving transistor T3 equals voltage of second voltage supply V2 less that of storage capacitor

Cs; i.e., $V_{g3} = V2 - V_{cs}$.

Drive current passing through driving transistor T3 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{sg3} - V_{th3})^2$ and $V_{sg3} = VDD - V_{g3} = VDD - (V2 - V_{cs})$. Luminescence device 40 is
5 illuminated as drive current (I_{Drive}) passes through it via connect transistor T4.

In summary, the relationship between data current (I_{Data}) and drive current (I_{Drive}) is shown as $I_{Drive} = (1/2) \times \beta \times [(2 \times I_{Data} / \beta)^{(1/2)} + V1 - V2]^2$.

10 According to the above theory and formula, current output to luminescence device 40 is only related to data current (I_{Data}) written, not threshold voltage (V_{th}) of driving transistor T3. As a result, threshold voltage difference resulted from process factors can be
15 compensated.

Voltage difference between first voltage supply V1 and second voltage supply V2 causes an offset at gate(G) voltage (V_{g3}) of driving transistor T3. If voltage of second voltage supply V2 is greater than that of first
20 voltage supply V1, larger data current (I_{Data}) may be imported by small drive current (I_{Drive}) at low gray scale to reduce charging time of storage capacitor Cs and parasitical capacitor.

Embodiment 2:

25 Refer to Fig.2 for the circuit of a pixel of embodiment

2 in this invention. As the Figure shows, the driving circuit of each pixel on the display panel includes one scan line 10 and one data line 20. The driving circuit in this embodiment is about the same as that in Embodiment 1; however, the only difference is source (S) of first switch transistor T5 connected to emission line 30 instead of first voltage supply V1 and source (S) of second switch transistor T6 connected to scan line 10, not second voltage supply V2.

10 Actuation procedures of Embodiment 2 are described as follows:

1. When the system scans the nth scan line 10, the potential is low ($V_{S,L}$), leading first scan transistor T1, second scan transistor T2 and first switch transistor T5 to become on. As the potential of the nth emission line 30 is high ($V_{E,H}$), connect transistor T4 and second switch transistor T6 are off. Thus, no current will pass through luminescence device 40 to prevent writing mistakes to the storage capacitor Cs.

20 One end of storage capacitor Cs connected to gate(G) of driving transistor T3 links up with data line 20 through first scan transistor T1 and the other end is connected to nth emission line 30 via first switch transistor T5. Meanwhile, part of data current (I_{Data}) charges/discharges storage capacitor Cs through first scan transistor T1 and

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first switch transistor T5. Gate voltage (V_{g3}) of driving transistor T3 equals voltage of emission line 30 ($V_{E,H}$) less that of storage capacitor Cs ($V_{E,H} - V_{CS}$).

Consequently, drive current (I_{Drive}) passing through driving transistor T3 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{sg3} - V_{th3})^2$ (β as trans-conductance parameter of driving transistor T3 and source gate voltage of driving transistor T3, $V_{sg3} = VDD - V_{g3} = VDD - (V_{E,H} - V_{CS})$). Hence, data current I_{Data} equals current passing through storage capacitor Cs (I_{CS}) plus drive current (I_{Drive}) passing through driving transistor T3; i.e., $I_{Data} = I_{CS} + I_{Drive}$.

2. Voltage of storage capacitor Cs (V_{CS}) makes drive current (I_{Drive}) passing through driving transistor T3 the same as data current (I_{Data}) of data line 20; that is, $I_{Data} = I_{Drive} = (1/2) \times \beta \times (V_{sg3} - V_{th3})^2$ and $V_{sg3} = VDD - V_{g3} = VDD - (V_{E,H} - V_{CS})$.

Data write is completed at the moment and voltage of storage capacitor Cs (V_{CS}) = $(2 \times I_{Data} / \beta)^{(1/2)} - (VDD - V_{E,H} - V_{th3})$.

3. Lastly, when the potential of the nth scan line changes from low ($V_{S,L}$) to high ($V_{S,H}$), first scan transistor T1, second scan transistor T2 and first switch transistor T5 are OFF. Meanwhile, potential of the nth emission line 30 changes from high ($V_{E,H}$) to low ($V_{E,L}$), leading connect transistor T4 and second switch

transistor T6 are ON.

One end of storage capacitor Cs is connected to gate (G) of driving transistor T3 and the other end to scan line 10 via second switch transistor T6. Thus, gate voltage V_{g3} of driving transistor T3 equals voltage of scan line 10 at high potential ($V_{S,H}$) less that of storage capacitor Cs; i.e., $V_{g3} = V_{S,H} - V_{cs}$.

Drive current passing through driving transistor T3 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{sg3} - V_{th3})^2$ and $V_{sg3} = VDD - V_{g3} = VDD - (V_{S,H} - V_{CS})$. Luminescence device 40 is illuminated as drive current (I_{Drive}) passes through it via connect transistor T4.

In summary, the relationship between data current (I_{Data}) and drive current (I_{Drive}) is shown as $I_{Drive} = (1/2) \times \beta \times [(2 \times I_{Data} / \beta)^{(1/2)} + V_{E,H} - V_{S,H}]^2$.

According to the above theory and formula, current output to luminescence device 40 is only related to data current (I_{Data}) written, not threshold voltage (V_{th}) of driving transistor T3. As a result, threshold voltage difference resulting from processing factors can be compensated for.

In addition, voltage differences between scan line 10 ($V_{S,H}$) high level voltage and emission line 30 ($V_{E,H}$) high level voltage causes an offset at gate (G) voltage (V_{g3}) of driving transistor T3. If potential of scan line 10 ($V_{S,H}$)

is higher than that of emission line 30 ($V_{E,H}$), greater data current (I_{Data}) may be imported by small drive current (I_{Drive}) at low gray scale to reduce charging time of storage capacitor C_s and parasitical capacitor.

5 Embodiment 3:

Refer to Fig.3 for the circuit of a pixel of embodiment 3 in this invention. As the Figure shows, the driving circuit of each pixel on the display panel includes one scan line 10 and one data line 20. The driving circuit in
10 this embodiment is about the same as that in Embodiment 1; however, the only difference is the source (S) of first switch transistor T5 is connected to voltage supply VDD instead of First voltage supply V1 and source (S) of second switch transistor T6 still connected to second
15 voltage supply V2 as in Embodiment 1.

Actuation procedures of Embodiment 3 are described as follows:

1. When the system scans the nth scan line 10, the potential is low ($V_{S,L}$), leading first scan transistor T1, second scan transistor T2 and first switch transistor T5 to
20 become on. As the potential of the nth emission line 30 is high ($V_{E,H}$), connect transistor T4 and second switch transistor T6 are off. Thus, no current will pass through luminescence device 40 to prevent writing mistakes of
25 storage capacitor C_s .

One end of storage capacitor C_s connected to gate of driving transistor T3 links up with data line 20 through scan transistor T1 and the other end is connected to voltage supply VDD via first switch transistor T5.

5 Meanwhile, part of data current (I_{Data}) charges/discharges storage capacitor C_s through first scan transistor T1 and first switch transistor T5. Gate voltage (V_{g3}) of driving transistor T3 equals voltage of voltage supply VDD less that of storage capacitor C_s ($V_{DD} - V_{CS}$).

10 Consequently, drive current (I_{Drive}) passing through driving transistor T3 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{sg3} - V_{th3})^2$ (β as trans-conductance parameter of driving transistor T3 and source gate voltage of driving transistor T3, $V_{sg3} = V_{DD} - V_{g3} = V_{DD} - (V_{DD} - V_{CS})$). Hence, data
15 current (I_{Data}) equals current passing through storage capacitor C_s (I_{CS}) plus drive current (I_{Drive}) passing through driving transistor T3; i.e., $I_{Data} = I_{CS} + I_{Drive}$.

2. Voltage of storage capacitor C_s (V_{CS}) makes drive current (I_{Drive}) passing through driving transistor T3 the
20 same as data current (I_{Data}) of data line 20; that is, $I_{Data} = I_{Drive} = (1/2) \times \beta \times (V_{sg3} - V_{th3})^2$ and $V_{sg3} = V_{DD} - V_{g3} = V_{DD} - (V_{DD} - V_{CS})$.

Data write is completed at the moment and voltage of storage capacitor C_s (V_{CS}) = $(2 \times I_{Data} / \beta)^{(1/2)} - (V_{DD} - V_{th3})$.
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3. Last, when potential of the nth scan line 10 changes from low ($V_{S,L}$) to high ($V_{S,H}$), first scan transistor T1, second scan transistor T2 and first switch transistor T5 are off. Meanwhile, potential of the nth emission line 30 changes from high ($V_{E,H}$) to low ($V_{E,L}$), leading connect transistor T4 and second switch transistor T6 to become on.

One end of storage capacitor Cs is connected to gate of driving transistor T3 and the other end to second voltage supply V2 via second switch transistor T6. Thus, gate voltage (V_{g3}) of driving transistor T3 equals voltage of second voltage supply V2 less that of storage capacitor Cs; i.e., $V_{g3} = V2 - V_{cs}$.

Drive current passing through driving transistor T3 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{sg3} - V_{th3})^2$ and $V_{sg3} = VDD - V_{g3} = VDD - (V2 - V_{cs})$. Luminescence device 40 is illuminated as drive current (I_{Drive}) passes through it via connect transistor T4.

In summary, the relationship between data current (I_{Data}) and drive current (I_{Drive}) is shown as $I_{Drive} = (1/2) \times \beta \times [(2 \times I_{Data} / \beta)^{(1/2)} + VDD - V2]^2$.

According to the above theory and formula, current output to luminescence device 40 is only related to data current (I_{Data}) written, not threshold voltage (V_{th}) of driving transistor T3. As a result, threshold voltage

difference resulted from process factors can be compensated.

In addition, voltage difference between voltage supply VDD and second voltage supply V2 causes an offset at the gate (G) of driving transistor T3. If voltage of second voltage supply V2 is greater than that of voltage supply VDD, larger data current (I_{Data}) may be imported by small drive current (I_{Drive}) at low gray scale to reduce charging time of storage capacitor Cs and parasitical capacitor.

Embodiment 4:

Refer to Fig.4 for the circuit of a pixel of embodiment 4 in this invention. As the Figure shows, the driving circuit of each pixel on the display panel includes one scan line 10 and one data line 20. The driving circuit in this embodiment is about the same as that in Embodiment 2; however, the only difference is source (S) of first switch transistor T5 connected to voltage supply VDD instead of emission line 30 and source (S) of second switch transistor T6 still connected to scan line 10.

Actuation procedures of Embodiment 4 are described as follows:

1. When the systems scans the nth scan line 10, the potential is low ($V_{S,L}$), leading first scan transistor T1, second scan transistor T2 and first switch transistor T5 to

become on. As the potential of the nth emission line 30 is high ($V_{E,H}$), connect transistor T4 and second switch transistor T6 are OFF. Thus, no current will pass through luminescence device 40 to prevent writing mistakes of storage capacitor Cs.

One end of storage capacitor Cs connected to gate(G) of driving transistor T3 links up with data line 20 through scan transistor T1 and the other end is connected to voltage supply VDD via first switch transistor T5. Meanwhile, part of data current (I_{Data}) charges/discharges storage capacitor Cs through first scan transistor T1 and first switch transistor T5. Gate voltage (V_{g3}) of driving transistor T3 equals voltage of voltage supply VDD less that of storage capacitor Cs ($VDD - V_{CS}$).

Consequently, drive current (I_{Drive}) passing through driving transistor T3 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{sg3} - V_{th3})^2$ (β as trans-conductance parameter of driving transistor T3 and source gate voltage of driving transistor T3, $V_{sg3} = VDD - V_{g3} = VDD - (VDD - V_{CS})$). Hence, data current (I_{Data}) equals current passing through storage capacitor Cs (I_{CS}) plus drive current (I_{Drive}) passing through driving transistor T3; i.e., $I_{Data} = I_{CS} + I_{Drive}$.

2. Voltage of storage capacitor Cs (V_{CS}) makes drive current (I_{Drive}) passing through driving transistor T3 the same as data current (I_{Data}) of data line 20; that is, $I_{Data} =$

$$I_{\text{Drive}} = (1/2) \times \beta \times (V_{\text{sg3}} - V_{\text{th3}})^2 \text{ and } V_{\text{sg3}} = V_{\text{DD}} - V_{\text{g3}} = V_{\text{DD}} - (V_{\text{DD}} - V_{\text{CS}}).$$

Data write is completed at the moment and voltage of storage capacitor C_s (V_{CS}) = $(2 \times I_{\text{Data}} / \beta)^{(1/2)} - (V_{\text{DD}} - V_{\text{DD}} - V_{\text{th3}})$.

3. Last, when potential of the n th scan line 10 changes from low ($V_{\text{S,L}}$) to high ($V_{\text{S,H}}$), first scan transistor T1, second scan transistor T2 and first switch transistor T5 are off. Meanwhile, potential of the n th emission line 30 changes from high ($V_{\text{E,H}}$) to low ($V_{\text{E,L}}$), leading connect transistor T4 and second switch transistor T6 to become on.

One end of storage capacitor C_s is connected to gate (G) of driving transistor T3 and the other end to scan line 10 via second switch transistor T6. Thus, gate voltage (V_{g3}) of driving transistor T3 equals voltage of scan line 10 at high ($V_{\text{S,H}}$) less that of storage capacitor C_s ; i.e., $V_{\text{g3}} = V_{\text{S,H}} - V_{\text{CS}}$.

Drive current passing through driving transistor T3 is as follows: $I_{\text{Drive}} = (1/2) \times \beta \times (V_{\text{sg3}} - V_{\text{th3}})^2$ and $V_{\text{sg3}} = V_{\text{DD}} - V_{\text{g3}} = V_{\text{DD}} - (V_{\text{S,H}} - V_{\text{CS}})$. Luminescence device 40 is illuminated as drive current (I_{Drive}) passes through it via connect transistor T4.

In summary, the relationship between data current (I_{Data}) and drive current (I_{Drive}) is shown as $I_{\text{Drive}} =$

$$(1/2) \times \beta \times [(2 \times I_{\text{Data}} / \beta)^{(1/2)} + V_{\text{DD}} - V_{\text{S,H}}]^2.$$

According to the above theory and formula, current output to luminescence device 40 is only related to data current (I_{Data}) written, not threshold voltage (V_{th}) of driving transistor T3. As a result, threshold voltage difference resulting from processing factors can be compensated.

In addition, voltage differences between voltage supply VDD and scan line 10 high level voltage causes an offset at the gate (G) of driving transistor T3. If the voltage of scan line 10 ($V_{\text{S,H}}$) is greater than that of voltage supply VDD, larger data current (I_{Data}) may be imported by small drive current (I_{Drive}) at low gray scale to reduce charging time of storage capacitor Cs and parasitical capacitor.

Embodiment 5:

Refer to Fig.5 for the circuit of a pixel of embodiment 5 in this invention. As the Figure shows, the driving circuit of each pixel on the display panel includes one scan line 10 and one data line 20 as follows:

Gates (G) of a first scan transistor N1 and a second scan transistor N2 connected to one scan line 10 and source (S) connected to a data line 20.

Source (S) of a driving transistor N3 is grounded.
Source (S) of one connect transistor N4 connected to

drains (D) of driving transistor N3 and first scan transistor N1 and gate (G) connected to one emission line 30.

Source (S) of a first switch transistor N5 connected
5 to first voltage supply V1 and gate(G) connected to scan line 10. Source (S) of a second switch transistor N6 connected to second voltage supply V2 and gate (G) connected to emission line 30. The above first scan transistor N1, second scan transistor N2, driving
10 transistor N3, connect transistor N4, first switch transistor N5 and second switch transistor N6 are NMOS transistors.

One end of the storage capacitor Cs is connected to the drains of the first switch transistor N5 and second
15 switch transistor N6 and the other end connected to drain (D) of second scan transistor N1 and gate (G) of driving transistor N3. Anode of a luminescence device 40 connected to voltage supply VDD and cathode connected to drain of connect transistor N4. Luminescence device
20 40 is an electro-luminescence device (EL device).

Gate (G) of connect transistor N4 controlled by nth emission line 30 and current passing through luminescence device 40 determined by gate (G) voltage of driving transistor N3.

25 Gate(G) of first switch transistor N5 also controlled

by nth scan line 10. Gate (G) of second switch transistor N6 controlled by nth emission line 30.

It is different from Embodiment 1 in that one end of luminescence device 40 is connected to voltage supply VDD and the other end to connect transistor N4. Furthermore, first scan transistor N1, second scan transistor N2, driving transistor N3, connect transistor N4, first switch transistor N5 and second switch transistor N6 are NMOS transistors.

Actuation procedures of Embodiment 5 are described as follows:

1. When the systems scans the nth scan line 10, the potential is high ($V_{S,H}$), leading first scan transistor N1, second scan transistor N2 and first switch transistor N5 to become on. As the potential of the nth emission line 30 is low ($V_{E,L}$), connect transistor N4 and second switch transistor N6 are off. Thus, no current will pass through luminescence device 40 to prevent writing mistakes to the storage capacitor Cs.

One end of storage capacitor Cs connected to gate of driving transistor N3 links up with data line 20 through second scan transistor N2 and the other end is connected to first voltage supply V1 via first switch transistor N5. Meanwhile, part of data current (I_{Data}) of data line 20 charges/discharges storage capacitor Cs through first scan

transistor N1 and first switch transistor N5. Gate voltage (V_{g3}) of driving transistor N3 equals voltage of first voltage supply V1 less that of storage capacitor Cs ($V1 + V_{CS}$).

5 Consequently, drive current (I_{Drive}) passing through driving transistor N3 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{gs3} - V_{th3})^2$ (β as trans-conductance parameter of driving transistor N3 and source gate voltage of driving transistor N3, $V_{gs3} = V_{g3} = V1 + V_{CS}$). Hence, data current (I_{Data})
10 equals current passing through storage capacitor Cs (I_{CS}) plus drive current (I_{Drive}) passing through driving transistor N3; i.e., $I_{Data} = I_{CS} + I_{Drive}$.

2. Voltage of storage capacitor Cs (V_{CS}) makes drive current (I_{Drive}) passing through driving transistor N3 the
15 same as data current (I_{Data}) of data line 20; that is, $I_{Data} = I_{Drive} = (1/2) \times \beta \times (V_{gs3} - V_{th3})^2$ and $V_{gs3} = V_{g3} = V1 + V_{CS}$.

Data write is completed at the moment and voltage of storage capacitor Cs (V_{CS}) = $(2 \times I_{Data} / \beta)^{(1/2)} - (V1 - V_{th3})$.

3. Last, when potential of the nth scan line 10 changes
20 from high ($V_{S,H}$) to low ($V_{S,L}$), first scan transistor N1, second scan transistor N2 and first switch transistor N5 are off. Meanwhile, potential of the nth emission line 30 changes from low ($V_{E,L}$) to high ($V_{E,H}$), leading connect transistor N4 and second switch transistor N6 to ON.

25 One end of storage capacitor Cs is connected to gate

of driving transistor N3 and the other end to second voltage supply V2 via second switch transistor N6. Thus, gate (G) voltage (V_{g3}) of driving transistor N3 is $V2 + V_{Cs}$. Drive current passing through driving transistor N3 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{gs3} - V_{th3})^2$ and $V_{gs3} = V_{g3} = V2 + V_{Cs}$. Luminescence device 40 is illuminated as drive current (I_{Drive}) passes through it via connect transistor N4.

In summary, the relationship between data current (I_{Data}) and drive current (I_{Drive}) is shown as $I_{Drive} = (1/2) \times \beta \times [(2 \times I_{Data} / \beta)^{(1/2)} + V2 - V1]^2$.

According to the above theory and formula, current output to luminescence device 40 is only related to data current (I_{Data}) written, not threshold voltage (V_{th}) of driving transistor N3. As a result, threshold voltage difference resulted from process factors can be compensated.

In addition, voltage difference between second voltage supply V2 and first voltage supply V1 causes an offset at the gate of driving transistor N3. If voltage of second voltage supply V2 is less than that of first voltage supply V1, larger data current (I_{Data}) may be imported by small drive current (I_{Drive}) at low gray scale to reduce the long charging time of storage capacitor Cs and parasitical capacitor.

Embodiment 6:

Refer to Fig.6 for the circuit of a pixel of embodiment 6 in this invention. As the Figure shows, the driving circuit of each pixel on the display panel includes one scan line 10 and one data line 20. The driving circuit in this embodiment is about the same as that in Embodiment 5; however, the only difference is source (S) of first switch transistor N5 connected to emission line 30 instead of first voltage supply V1 and source (S) of second switch transistor N6 connected to scan line 10 instead of second voltage supply V2.

Actuation procedures of Embodiment 6 are described as follows:

1. When the systems scans the nth scan line 10, the potential is high ($V_{S,H}$), leading first scan transistor N1, second scan transistor N2 and first switch transistor N5 to become on. As the potential of the nth emission line 30 is low ($V_{E,L}$), connect transistor N4 and second switch transistor N6 are OFF. Thus, no current will pass through luminescence device 40 to prevent writing mistakes to the storage capacitor Cs.

One end of storage capacitor Cs connected to gate of driving transistor N3 links up with data line 20 through second scan transistor N2 and the other end is connected to nth emission line 30 via first switch transistor N5.

Meanwhile, part of data current (I_{Data}) of data line 20 charges/discharges storage capacitor C_s through first scan transistor N1 and first switch transistor N5. Gate voltage (V_{g3}) of driving transistor N3 equals low voltage of nth emission line 30 less that of storage capacitor C_s (V_{CS}); i.e., $V_{g3} = V_{E,L} + V_{CS}$.

Consequently, drive current (I_{Drive}) passing through driving transistor N3 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{gs3} - V_{th3})^2$ (β as trans-conductance parameter of driving transistor N3 and source gate voltage of driving transistor N3, $V_{gs3} = V_{g3} = V_{E,L} + V_{CS}$. Hence, data current (I_{Data}) equals current passing through storage capacitor C_s (I_{CS}) plus drive current (I_{Drive}) passing through driving transistor N3; i.e., $I_{Data} = I_{CS} + I_{Drive}$.

2. Voltage of storage capacitor C_s (V_{CS}) makes drive current (I_{Drive}) passing through driving transistor N3 the same as data current (I_{Data}) of data line 20; that is, $I_{Data} = I_{Drive} = (1/2) \times \beta \times (V_{gs3} - V_{th3})^2$ and $V_{gs3} = V_{g3} = V_{E,L} + V_{CS}$.

Data write is completed at the moment and voltage of storage capacitor C_s , $V_{CS} = (2 \times I_{Data} / \beta)^{(1/2)} - (V_{E,L} - V_{th3})$.

3. Last, when potential of the nth scan line 10 changes from high ($V_{S,H}$) to low ($V_{S,L}$), first scan transistor N1, second scan transistor N2 and first switch transistor N5 are off. Meanwhile, potential of the nth emission line 30 changes from low ($V_{E,L}$) to high ($V_{E,H}$), leading connect

transistor N4 and second switch transistor N6 to become on.

One end of storage capacitor C_s is connected to gate (G) of driving transistor N3 and the other end to scan line 10 via second switch transistor N6. Thus, gate (G) voltage (V_{g3}) of driving transistor N3 is $V_{S,L} + V_{Cs}$. Drive current passing through driving transistor N3 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{gs3} - V_{th3})^2$ and $V_{gs3} = V_{g3} = V_{S,L} + V_{Cs}$. Luminescence device 40 is illuminated as drive current (I_{Drive}) passes through it via connect transistor N4.

In summary, the relationship between data current (I_{Data}) and drive current (I_{Drive}) is shown as $I_{Drive} = (1/2) \times \beta \times [(2 \times I_{Data} / \beta)^{(1/2)} + V_{S,L} - V_{E,H}]^2$.

According to the above theory and formula, current output to luminescence device 40 is only related to data current (I_{Data}) written and not the threshold voltage (V_{th}) of driving transistor N3. As a result, threshold voltage difference resulted from process factors can be compensated.

In addition, voltage differences between scan line 10 ($V_{S,L}$) low level voltage and emission line 30 ($V_{E,L}$) low level voltage causes an offset at the gate of driving transistor N3. If the voltage of scan line 10 ($V_{S,L}$) is less than that of emission line 30 ($V_{E,L}$), larger data current

(I_{Data}) may be imported by small drive current (I_{Drive}) at low gray scale to reduce the long charging time of storage capacitor C_s and parasitical capacitor.

Embodiment 7:

5 Refer to Fig.7 for the circuit of a pixel of embodiment 7 in this invention. As the Figure shows, the driving circuit of each pixel on the display panel includes one scan line 10 and one data line 20. The driving circuit in this embodiment is about the same as that in Embodiment 10 5; however, the only difference is source (S) of first switch transistor N5 grounded instead of connecting to first voltage supply V1 and source (S) of second switch transistor T6 still connected to second voltage supply V2 as in Embodiment 5.

15 Actuation procedures of Embodiment 7 are described as follows:

1. When the systems scans the n th scan line 10, the potential is high ($V_{S,H}$), leading first scan transistor N1, second scan transistor N2 and first switch transistor N5 to 20 ON. As the potential of the n th emission line 30 is low ($V_{E,L}$), connect transistor N4 and Second switch transistor N6 are off. Thus, no current will pass through luminescence device 40 in this phase to prevent writing mistakes to the storage capacitor C_s .

25 One end of storage capacitor C_s connected to gate of

driving transistor N3 links up with data line 20 through second scan transistor N2 and the other end is grounded via first switch transistor N5. Meanwhile, part of data current (I_{Data}) of data line 20 charges/discharges storage capacitor C_s through first scan transistor N1 and first switch transistor N5. Gate voltage (V_{g3}) of driving transistor N3 equals voltage of storage capacitor C_s (V_{CS}); i.e., $V_{g3} = 0 + V_{CS}$.

Consequently, drive current (I_{Drive}) passing through driving transistor N3 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{gs3} - V_{th3})^2$ (β as trans-conductance parameter of driving transistor N3 and source gate voltage of driving transistor N3, $V_{gs3} = V_{g3} = 0 + V_{CS}$. Hence, data current (I_{Data}) equals current passing through storage capacitor C_s (I_{CS}) plus drive current (I_{Drive}) passing through driving transistor N3; i.e., $I_{Data} = I_{CS} + I_{Drive}$.

2. Voltage of Storage Capacitor C_s (V_{CS}) makes drive current (I_{Drive}) passing through Driving transistor N3 the same as data current (I_{Data}) of Data Line 20; that is, $I_{Data} = I_{Drive} = (1/2) \times \beta \times (V_{gs3} - V_{th3})^2$ and $V_{gs3} = V_{g3} = 0 + V_{CS}$.

Data write is completed at the moment and voltage of storage capacitor C_s , $V_{CS} = (2 \times I_{Data} / \beta)^{(1/2)} - (0 - V_{th3})$.

3. Lastly, when the potential of the n th scan line changes from high ($V_{S,H}$) to low ($V_{S,L}$), first scan transistor N1, second scan transistor N2 and first switch

transistor N5 are off. Meanwhile, potential of the nth emission line 30 changes from low ($V_{E,L}$) to high ($V_{E,H}$), leading connect transistor N4 and second switch transistor N6 to become on.

5 One end of storage capacitor C_s is connected to gate (G) of driving transistor N3 and the other end to second voltage supply V2 via second switch transistor N6. Thus, gate voltage (V_{g3}) of driving transistor N3 is $V_2 + V_{Cs}$. Drive current passing through driving transistor N3
 10 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{gs3} - V_{th3})^2$ and $V_{gs3} = V_{g3} = V_2 + V_{Cs}$. Luminescence device 40 is illuminated as drive current (I_{Drive}) passes through it via connect transistor N4.

In summary, the relationship between data current
 15 (I_{Data}) and drive current (I_{Drive}) is shown as $I_{Drive} = (1/2) \times \beta \times [(2 \times I_{Data} / \beta)^{(1/2)} + V_2 - 0]^2 = (1/2) \times \beta \times [(2 \times I_{Data} / \beta)^{(1/2)} + V_2]^2$.

According to the above theory and formula, current output to luminescence device 40 is only related to data
 20 current (I_{Data}) written, not threshold voltage (V_{th}) of driving transistor N3. As a result, threshold voltage difference resulted from process factors can be compensated.

In addition, voltage difference between second
 25 voltage supply V2 and grounding (0) causes an offset at

the gate of driving transistor N3. If voltage of second voltage supply V2 is less than that of grounding (0), larger data current (I_{Data}) may be imported by small drive current (I_{Drive}) at low gray scale to reduce long charging
5 time of storage capacitor Cs and parasitical capacitor.

Embodiment 8:

Refer to Fig.8 for the circuit of a pixel of embodiment 8 in this invention. As the Figure shows, the driving circuit of each pixel on the display panel includes one
10 scan line 10 and one data line 20. The driving circuit in this embodiment is about the same as that in Embodiment 6; however, the only difference is source (S) of first switch transistor N5 is grounded instead of connecting to emission line 30 and source (S) of second switch
15 transistor T6 still connected to scan line 10 as in Embodiment 6.

Actuation procedures of Embodiment 8 are described as follows:

1. When the systems scans the nth scan line 10, the
20 potential is high ($V_{S,H}$), leading first scan transistor N1, second scan transistor N2 and first switch transistor N5 to become on. As the potential of the nth emission line 30 is low ($V_{E,L}$), connect transistor N4 and second switch transistor N6 are OFF. Thus, no current will pass through
25 luminescence device 40 in this phase to prevent writing

mistakes to the storage capacitor C_s .

One end of storage capacitor C_s connected to gate of driving transistor N3 links up with data line 20 through second scan transistor N2 and the other end is grounded via first switch transistor N5. Meanwhile, part of data current (I_{Data}) of data line 20 charges/discharges storage capacitor C_s through first scan transistor N1 and first switch transistor N5. Gate voltage (V_{g3}) of driving transistor N3 equals voltage of storage capacitor C_s (V_{CS}); i.e., $V_{g3} = 0 + V_{CS}$.

Consequently, drive current (I_{Drive}) passing through driving transistor N3 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{gs3} - V_{th3})^2$ (β as trans-conductance parameter of driving transistor N3 and source gate voltage of driving transistor N3, $V_{gs3} = V_{g3} = 0 + V_{CS}$. Hence, data current (I_{Data}) equals current passing through storage capacitor C_s (I_{CS}) plus drive current (I_{Drive}) passing through driving transistor N3; i.e., $I_{Data} = I_{CS} + I_{Drive}$.

2. Voltage of storage capacitor C_s (V_{CS}) makes drive current (I_{Drive}) passing through driving transistor N3 the same as data current (I_{Data}) of data line 20; that is, $I_{Data} = I_{Drive} = (1/2) \times \beta \times (V_{gs3} - V_{th3})^2$ and $V_{gs3} = V_{g3} = 0 + V_{CS}$.

Data write is completed at the moment and voltage of Storage Capacitor C_s , $V_{CS} = (2 \times I_{Data} / \beta)^{(1/2)} - (0 - V_{th3})$.

3. Lastly, when potential of the nth Scan Line 10

changes from high ($V_{S,H}$) to low ($V_{S,L}$), first scan transistor N1, second scan transistor N2 and first switch transistor N5 are OFF. Meanwhile, potential of the nth emission line 30 changes from low ($V_{E,L}$) to high ($V_{E,H}$),
 5 leading connect transistor N4 and second switch transistor N6 to ON.

One end of storage capacitor C_s is connected to gate of driving transistor N3 and the other end to nth scan line
 10 via second switch transistor N6. Thus, gate voltage (V_{g3}) of driving transistor N3 is $V_{S,L} + V_{Cs}$. Drive current passing through driving transistor N3 is as follows: $I_{Drive} = (1/2) \times \beta \times (V_{gs3} - V_{th3})^2$ and $V_{gs3} = V_{g3} = V_{S,L} + V_{Cs}$. Luminescence device 40 is illuminated as drive current (I_{Drive}) passes through it via connect transistor N4.

15 In summary, the relationship between data current (I_{Data}) and drive current (I_{Drive}) is shown as $I_{Drive} = (1/2) \times \beta \times [(2 \times I_{Data} / \beta)^{(1/2)} + V_{S,L} - 0]^2 = (1/2) \times \beta \times [(2 \times I_{Data} / \beta)^{(1/2)} + V_{S,L}]^2$.

According to the above theory and formula, current
 20 output to luminescence device 40 is only related to data current (I_{Data}) written, not threshold voltage (V_{th}) of driving transistor N3. As a result, threshold voltage difference resulted from process factors can be compensated.

25 In addition, voltage difference between scan line 10

($V_{S,L}$) low level voltage and grounding ($V=0$) causes an offset at the gate of driving transistor N3. If voltage of scan line 10 ($V_{S,L}$) is less than that of grounding (0), larger data current (I_{Data}) may be imported by small drive
5 current (I_{Drive}) at low gray scale to reduce long charging time of storage capacitor C_s and parasitical capacitor.

To conclude, the Active Matrix Display Driving Circuit presented by this invention has the following advantages:

10 1. In comparison with the U.S. Pat. Nos. 6,373,454 and 6,229,506, the ratio of input current to output current in this invention can be shown as: output current = $A \times$ input current + B. It solves long charging/discharging time efficiently.

15 2. In comparison with the U.S. Pat. Nos. 6,359,605, 6,501,466 and 6,535,185, the correlation between input current and output current (output current = $A \times$ input current + B) is based on capacitive coupling, not the structure of current mirror. The issue of matching TFT
20 elements is not considered necessary. Consequently, influential process factors are reduced and the yield of panels increases.

3. In comparison with the above patented circuits, capacitive coupling exactly ensures source gate voltage
25 (V_{gs}) of the driving transistor be smaller than threshold

voltage (V_{th}), which generates no current for the driving transistor. In this way, the luminescence device won't be illuminated and a higher contrast is developed.

4. To compare with the thesis published by Samsung
5 with the subject of A New Current Programmable Pixel
Structure for large-Size and High-Resolution AMOLEDs
(International Display Workshops 2002 (IDW 2002)):

a. As only one capacitor is applied to achieve the
correlation ($\text{output current} = A \times \text{input current} + B$) in
10 this invention, voltage of capacitive coupling does not
change with relative values of two capacitors due to
process or/and layout effect, and driving transistor affect
the driving current. Consequently, influential process
factors are reduced and the yield of panels increases.

15 b. As one capacitor and two levels are used to achieve
the correlation ($\text{output current} = A \times \text{input current} + B$)
in this invention instead of capacitive coupling by two
capacitors, precision of the capacitor is not required.
Hence, influential process factors are reduced and the
20 yield of panels increases.

c. Since merely one capacitor is utilized to achieve
the correlation ($\text{output current} = A \times \text{input current} + B$)
in this invention, a higher aperture ratio is developed.

5. In comparison with general voltage driving circuits,
25 this invention is a current driving circuit that solves the

problem of different properties of TFT elements and compensates threshold voltage (V_{th}) difference and mobility automatically.

- 5 6. To compare with voltage driving circuits, the current driving circuit in this invention can solve the IR drop problem of the voltage supply line.